

ABSTRACT

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5 A system and method for providing a command stream on a chip or in a computer system is disclosed. The system comprises a central processing unit (CPU), a controller coupled to the CPU and a memory coupled to the controller. The controller manages the memory. The system and method also includes a storage element coupled to the memory, the storage element being accessible by the CPU via the controller. The system and method in accordance with the present invention allows the controller to receive commands from the CPU and to manage the storage element, typically a first in first out (FIFO) buffer, and incorporates the storage element as part of the memory. In so doing, the system performance is significantly improved by providing a virtual FIFO buffer such that the CPU sees a FIFO buffer with a size equal to the size of the memory. The bandwidth of the bus between the controller and the memory is typically greater than that of the system bus. Hence the performance of the overall system is significantly improved. In addition, since the controller is the only device that has access to the memory, the bandwidth of the bus associated therewith is not divided between two devices. Further, since the controller is managing the storage

10 element, the overhead considerations that related to managing the read and write pointers of the storage element by the CPU are eliminated. Finally, a technique in accordance with the present invention is provided such that the controller determines whether the storage element must be emptied, rather than requiring the CPU to perform this function. Through these features, a

15 command stream can be provided efficiently on a chip or in a computer system.

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